IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) An apparatus for reducing a magnitude of a rate of current change of an integrated circuit, comprising:

a control stage that generates a control signal indicative of whether power consumption by the integrated circuit needs to be reduced; and

a counter stage that inputs the control signal and generates a plurality of ~~sequential~~ signals to a plurality of transistors, wherein the ~~plurality of transistors source current from a power supply~~plurality of signals sequentially disable the plurality of transistors to cause a gradual reduction in an amount of current sourced from a power terminal to a ground terminal of the integrated circuit.

2. (Canceled)

3. (Currently Amended) The apparatus of claim [[2]]1, wherein the counter stage enables the plurality of transistors when power consumption by the integrated circuit does not need to be reduced.

4. (Original) The apparatus of claim 1, wherein the plurality of transistors are each one selected from the group consisting of a p-type transistor and a n-type transistor.

5. (Currently Amended) A circuit for reducing a rate of current change of a microprocessor, comprising:

a control stage that is connected to a power terminal and a ground terminal, wherein the control stage generates a control signal that is indicative of whether power consumption by the microprocessor needs to be reduced; and

a counter stage that inputs the control signal and a clock signal, wherein the counter stage is arranged to generate[[s]] a ~~first signal to a gate terminal of a first transistor~~plurality of signals to a plurality of transistors connected in parallel across the power terminal and the ground terminal,

wherein, dependent on the control signal, the plurality of signals are generated to sequentially disable the plurality of transistors to cause a gradual reduction in an amount of current sourced from the power terminal to the ground terminal by the plurality of transistors.

6-10. (Canceled)

11. (New) The circuit of claim 5, wherein the plurality of transistors, when in an enabled state, source substantially a maximum amount of current from the power terminal to the ground terminal.